Abstract

A digital system and method of operation is provided in which the digital system has at least one processor (2000), with an associated multi-segment local memory circuit (2006). Validity circuitry (VI) is connected to the memory circuit and is operable to indicate if each segment of the plurality of segments holds valid data. Dirty bit circuitry (DI) is connected to the memory circuit for indicating if data within the local memory is incoherent with a secondary memory (2002). DMA circuitry (2030) can transfer (2041) blocks of data/instructions (2020) between the local memory and the secondary memory. The valid bits and dirty bits are set in response to DMA transfers. A mode circuit controls how DMA transfers are affected by the dirty bits. When the mode circuit is in a first mode, the DMA circuitry transfers an entire block from the local memory to the secondary memory. When the mode circuit is in a second mode, the DMA circuitry transfers only segments marked as being dirty. Transaction requests by the processor to locations within the local memory are stalled if the requested segment has not yet been loaded by a DMA transfer.